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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,977	MOK ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed May 15, 2006. Claims 1-10,14-17 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claims 1-10,14-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re base claims 1,14,15, meaning and scope of the claims are indefinite and unclear for whether these "circuit patterns" are the same, since "forming circuit patterns..." are already recited in substep (c) of step (A), but step (E) lately recites "thereafter, forming circuit patterns...".

Claim Rejections - 35 USC § 102

2. Claims 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Egitto et al (6,826,830).

Re claim 16, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: forming a plurality of circuit layers, wherein the circuit layers comprise via holes (Figs 19,24); forming a plurality of insulating layers, wherein the insulating layers comprises via holes filled with a conductive paste 555 (Figs 23-25; Fig 2); alternately arranging the circuit layers 560,570 and insulating layers 580 (Fig 24); and pressing the circuit layers and insulating layers and filling the via holes of the circuit layers with the conductive paste 555 from the via holes of the insulating layers to electrically connect the insulating layers with the circuit layers (Figs 24-25). Re claim 17, wherein the via holes 563 of the circuit layers are not filled with the plating or with conductive paste before pressing (Figs 24-25; col 32, line 23 through col 33).

Claim Rejections - 35 USC § 103

3. Claims 1,9,14,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egitto et al (6,826,830) taken with Furui et al (5,258,094).

Re claims 1, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes through a copper stack plate (Figs 19,24); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper (Fig 19, col 30 line 60 through col 31); and (c) forming circuit patterns on the copper stack plate (Fig 19); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes through a flat-type insulating material provided with release films 544,542 (Fig 21) attached to surfaces of the flat-type insulating material; (b) filling the via holes with a conductive paste 555 (Figs 23-25,2); and (c) removing the release films 544,542 from the flat-type insulating material (Fig 23); (C) alternately arranging the circuit layers 560,570 and the insulating layers 580 at predetermined positions (Figs 24,2); (D) connecting the insulating layers to the circuit layers, wherein the conductive paste 555 filling the via holes of the insulating layers flows into the via holes of the circuit layers by pressing the arranged circuit and insulating layers (Figs 24-25), wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25). Re claims 14, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes through a copper stack plate (Figs 19,24); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper (Fig 19, col 30 line 60 through col 31); and (c) forming circuit patterns on the copper stack plate (Fig 19); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes through a flat-type insulating material provided with release films 544,542 (Fig 21) attached to surfaces of the flat-type insulating material; (b) filling the via holes with a conductive paste 555 (Figs 23-25,2); and (c) removing the release films 544,542 from the flat-type insulating material (Fig 23); (C) alternately arranging the circuit layers 560,570 and the insulating layers 580 at predetermined positions (Figs 24,2); (D) pressing the arranged circuit

and insulating layers and filling the via holes in the circuit layers with conductive paste 555 from the insulating layers (Figs 24-25), wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25) . Re claims 15, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes through a copper stack plate (Figs 19,24); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper without completely filling the via holes (Fig 19, col 30 line 60 through col 31); and (c) forming circuit patterns on the copper stack plate (Fig 19); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes through a flat-type insulating material provided with release films 544,542 (Fig 21) attached to surfaces of the flat-type insulating material; (b) filling the via holes with a conductive paste 555 (Figs 23-25,2); and (c) removing the release films 544,542 from the flat-type insulating material (Fig 23); (C) alternately arranging the circuit layers 560,570 and the insulating layers 580 at predetermined positions (Figs 24,2); (D) pressing the arranged circuit and insulating layers (Figs 24-25); and wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25). Re claim 9, wherein the conductive paste functions as a point contact-type conductive paste 555 (Fig 23).

Egitto teaches forming circuit patterns 567,578 on the circuit layers, before pressing (Figs 24-25); whereas, base claims 1,14,15 recite a step of forming circuit patterns on the outermost layers of a board obtained by pressing.

However, Furui teaches (at Figs 14-18; col 5, line 38 through col 6) forming circuit patterns 68,61,21,26,66,67 (Fig 17) on the outermost layers of a board 1 obtained by pressing the circuit layers 14,15 and the insulating layers 52 (Figs 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Egitto by forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers, as taught by Furui. This is because of the desirability to form desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the

insulating layer, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection.

4. Claims 1,3-5,7-10,14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (2004/0194303) taken with Egitto et al (6,826,830) and Furui et al (5,258,094).

Re base claims 1,14,15,16, Kim teaches (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit board, comprising the steps of: (A) forming a predetermined number of circuit layers, including the sub-steps of: (a) forming via holes 304 through a copper stack plate 302/303 (Figs 3A-3B); (b) plating surfaces of the copper stack plate and inner walls of the via holes with copper 305 (Fig 1C); and (c) forming circuit patterns 306 on the copper stack plate (Fig 1d; paragraph 72; 306a-306c in Fig 7); (B) forming a predetermined number of insulating layers, including the sub-steps of: (a) forming via holes 504 through a flat-type insulating material provided with release films 502 attached to surfaces of the flat-type insulating material 503 (Figs 5A-5B); (b) filling the via holes with a conductive paste 505 (Fig 5C); and (c) removing the release films 502 the flat-type insulating material (Fig 5D; paragraphs 81-85); (C) alternately arranging the circuit layers and the insulating layers at predetermined positions (Fig 7, paragraphs 93-97); (D), wherein omitting the plugging process of the via holes 204 using the paste 206 is alternatively taught at (at paragraph 61; Figs 2D-2E), wherein by omitting or not fill the via holes 204 with plating or conductive paste 206 before pressing at Figs 7-8 (paragraphs 61-63,55-60), and connecting the insulating layers to the circuit layers pressing the arranged circuit layers with the via holes and the insulating layers having conductive paste (Fig 8); and wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d). Re claim 3, wherein surface-treatment of the copper stack plate 105 is performed so as to increase an adhering force (paragraphs 16, 21,24; Figs 1A-1E). Re claims 4-5, further comprising the step of: (F) forming a target hole at the position of a target guide mark, serving as a reference point of drilling, on the circuit layers and the insulating layers (re claim 4); and, re claim 5) wherein the sub-step (a) of each of the steps (A) and (B) includes the step of: (a') forming a guide hole at the same position, serving as a reference point of interlayer matching, on the circuit layers and the insulating layers (paragraphs 95-96; page 7,

right column, lines 7-18). Re claim 7, wherein the release film 502 a thickness of 20 to 30 microns (paragraph 82; Figs 5A-5B). Re claims 8-9, wherein the conductive paste is a metallic bond-type conductive paste 106/505 impregnated with a tin (Sn) component, or re claim 9, wherein the conductive paste is considered as a point contact-type conductive paste 106/505 (paragraphs 16,84). Re claim 10, wherein the flat-type insulating material includes a resin material in a c-stage, and resin layers in a b-stage respectively stacked on both surfaces of the resin material (paragraph 87; Figs 6A-6D,5A-5D). Re further claims 15, as similarly applied to claim 1 above, Kim also alternatively teaches (at paragraphs 60-61; Figs 2C-2E) about plating inner walls of the via holes with copper 205 without completely filling the via holes. Thereafter, as shown in Figure 7-8, arranging and pressing such circuit layers and the insulating layers are arranged and pressed to form a parallel multi-layer printed circuit board, wherein circuit patterns 306a-306c from the plated copper 305 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers (Figs 7,8, 3d).

Re claims 1,14,16, Kim lacks filling the via holes in the circuit layers with the conductive paste; and Re claims 1,14-16, after obtain a board by pressing, forming circuit patterns on the outermost layers of a board.

However, Egitto teaches (at Figs 13-25, col 29, line 47 through col 32; Fig 1-2; cols 4-18) connecting the insulating layers to the circuit layers, wherein the conductive paste 555 filling the via holes of the insulating layers flows into the via holes of the circuit layers by pressing the arranged circuit and insulating layers (Figs 24-25), wherein circuit patterns 567,578 are formed on the outermost layers of a board obtained by pressing the circuit layers and the insulating layer (Fig 24-25). Furui teaches (at Figs 14-18; col 5, line 38 through col 6) forming circuit patterns 68,61,21,26,66,67 (Fig 17) on the outermost layers of a board 1 obtained by pressing the circuit layers 14,15 and the insulating layers 52 (Figs 14-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layer printed circuit board of Kim by flowing conductive paste from the insulating layer into emptied via holes in the circuit layers, as taught by Egitto. This is because of the desirability to provide an electrical connection, wherein the conductive paste are flown into the via holes so that the layers can be effectively joined together. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-

layer printed circuit board of Kim by forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers, as taught by Furui. This is because of the desirability to form desired circuit patterns on the outermost layer of the board obtained by pressing the circuit layer and the insulating layer, wherein desired circuit patterns on the board can be subsequently formed and made for a particular circuit connection.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (2004/0194303) taken with Egitto et al (6,826,830) and Furui et al (5,258,094), as applied to claim 1 above and further of Hirose (6,613,986).

Kim and Egitto teach (at Figs 3A-8; paragraphs 65 through 96) a method for manufacturing a parallel multi-layer printed circuit as applied to claims 1,3-5,7-10 above.

Kim and Egitto lack mentioning buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste, after the step (C).

However, Hirose teaches (at Figs 24C-25B, col 29, lines 10-22; Figs 1A-2D; col 16, lines 46-55) to buffing a portion of the conductive paste, flowing out from the via holes of the outmost layer, so as to remove the protruding portion of the conductive paste.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to manufacture the printed circuit board of Kim and Egitto by buffing a portion of the conductive paste flowing out from the via holes of the outmost layer, as taught by Hirose. This is because of the desirability to remove the unwanted protruding portion of the conductive past flowing out form the via holes.

Response to Amendment

6. Applicant's remarks and amendment filed May 15, 2006 and March 07, 2006 with respect to pending claims have been considered but they are moot in view of the new ground(s) of rejection.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-102

Michael Trinh
Primary Examiner